Implementing FSMs with Counters

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Implementing FSMs with Counters

Implementing the BCD to Excess 3 FSM

Definitions and Functions

Latches

Implementation Strategies

Xilinx LCA Architecture

Implementing the BCD to Excess 3 FSM

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Design Case Study

Traffic Light Controller

Decomposition into three subsystems:

- Controller FSM
- Mean time between failures

- Short term/long term interval counter

- Car Sensor

- Output Decoders and Traffic Lights
Design Case Study

LCA-Based Implementation

Counter/Multiplexer Method:

4: MUX, 2 bit Up-counter

MUX has variables (4 state, 2 control)

but this is the kind of 6 variable function that can be implemented in 1 CLB

2nd CLB to implement TL - C and TL + C

but note that 74HC00 is really a function of TL, C, TS, Q`, Q0

1 CLB to implement this function of 5 variables

2 bit Counter: 2 functions of 3 variables (2 bit state + count)

Alto implemented in one CLB

Traffic light decoder: functions of 2 variables (Q`, Q0)

2 per CLB = 3 CLB for the decoder

Total = 5 CLB