1. (a)
3. (a) Mux implementation

(b) FSM + datapath

Assumptions: (1) User needs to press the load button to start the shift after the input.

(2) Before the next input, user has to wait at least 4 clock cycles.
States: Start $\rightarrow$ initialize the FSM
Shift $\rightarrow$ the shift register is performing shifting

Inputs: Load $\rightarrow$ User presses the load button to start the shifter
Ready $\rightarrow$ signal from datapath to indicate if the output is ready

Outputs: Shift $\rightarrow$ Keep shifting at each clock cycle until the output is ready

(c) 3(a) is faster since the time delay for the 4:1 mux is far less than that for the shift register.
3(b) uses more hardware.
If space and response time are the critical considerations, 3(a) yields the best design.